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A Single-Phase Hybrid Seventeen Level Multilevel Inverter Topology

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Abstract: **Inverters play a major role in electrical field and there have been many advancement in this context. Multilevel inverter is one among them. This study proposes a single phase seventeen level multilevel inverter. Here the dc sources will be coupled in a series/parallel configuration to distribute the load. A couple of switches and voltage sources will be used for producing a larger number of output level voltage. The harmonic content will be reduced by using the technique of hybrid modulation. Comparison in THD value is done for thirteen level and seventeen level topology and THD value improvement can be seen here. The simulation of the inverter is carried out in SIMULINK.**

Keywords- Hybrid modulation, Multilevel inverter

I. INTRODUCTION

The curiosity in the concept of inverters and the desire to learn more about them made us to choose this topic. The goal is to obtain greater output voltage level with little number of switches and dc sources. To draw low-distortion input current and share load current among many dc voltage source, reduce switching losses. Power electronic converters, which are observed everywhere in our daily life are grouped into different types. Inverters are one among them, which are mainly used for power conversion have a wide range of applications i.e., used in HVDC power transmission, domestic and industrial power system, UPS, drives, turbines, heaters etc.

Multilevel inverter concept is one of the advancement in this frame of reference. MLIs generate required output voltage by using dc voltage source and as the number of dc voltage source escalate; the output voltage reaches a sinusoidal waveform. MLIs have lower harmonic distortion and switching losses than two-level inverters (conventional inverters) and are engaged in high power and high voltage applications. MLIs have changed over time, with new configurations such as Diode-clamped, Flying capacitor, Switched series/parallel sources, Series connected switched sources, Packed U cell and cascaded bipolar switched cells. But these configurations have several drawbacks like requirement of clamping diodes, capacitors, additional and different class of dc voltage sources, lots of switches, sometimes requires a bidirectional switch which increases the complexity, no load sharing capability.

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Here we are going through a single-phase seventeen level MLI with few switches and dc voltage sources that have load sharing capacity by conducting parallel operation of dc voltage sources and reducing harmonic content utilizing hybrid modulation.

II. METHODOLOGY

The functional flow diagram of multilevel inverter is shown as below. The flow diagram comprises of three modules that is shown as below.

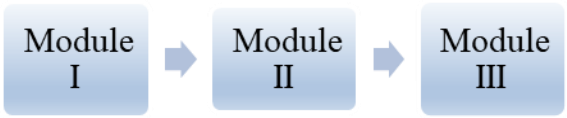

Figure 1: Functional flow diagram of Multilevel Inverter

Module I is made up of a certain number of cells. Three cells are used here, each of which contains one dc voltage source and three unidirectional switches. It generates a staircase waveform at the module's output from an additive mix of dc voltage sources.

If Sa1, Sa3 switches are both switched on, the voltage sources will be attached in parallel at the Vdc output. As a result, the cells share their load. If Sa2 is switched ON then dc sources will be connected with 2Vdcin series at the output. Switches (Sa1,Sa2) and (Sa2,Sa3) must work in complementary mode to confront short circuiting of voltage sources. Due to the series/parallel combination of dc voltage source, this module will not produce a zero level at the output.

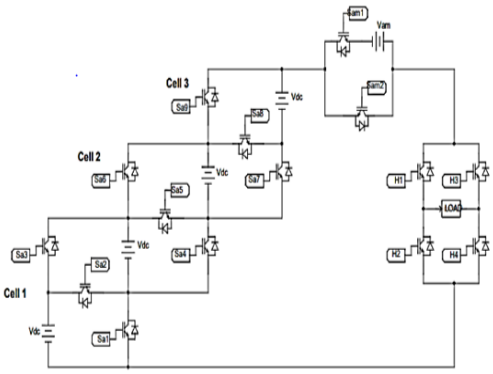

Figure 2: Circuit of Multilevel Inverter

Module II generates a larger number of levels. Two unidirectional switches and a dc voltage source make up

this circuit. Both switches must work in complementary mode to avoid short circuiting of the voltage source Vam.
When Sam2 switch is ON, same voltage at first module will appear at the output. When Sam1 is turned ON, Vam is added along with the voltage level generated by first module. If Vam is half of the dc source, an intermediary level will be obtained between the two levels. If Vam is equal to Vdc,no other levels will be formed.
Module III which is connected after second module, consists of H-bridge. Module I and II are used to produce only positive polarity so this third module is used to produce both the polarity voltage levels at the output and also to produce zero voltage level at the output.

a. Working

The MLI operation is explained with three cells (m = 3) in module I. For the three cells, the topology uses five dc sources and fifteen switches. Magnitude of voltage sources must be equal to accomplish parallel operation of dc voltage sources in module I.(Sa1,Sa2) and(Sa2, Sa3) forms the switch pairs of the cell.

Table 1: Switching table

	S1/S3	S2	S4/S6	S5	S7/S9	S8	Sa1	Sa2	H1	H2	H3	H4	Vo
1	0	0	0	0	0	0	0	0	0	1	0	1	0
2	1	0	1	0	1	0	0	1	1	0	0	1	Vdc
3	1	0	1	0	1	0	1	0	1	0	0	1	Vdc+Va
4	0	1	1	0	1	0	0	1	1	0	0	1	2Vdc
5	0	1	1	0	1	0	1	0	1	0	0	1	2Vdc+Va
6	0	1	0	1	1	0	0	1	1	0	0	1	3Vdc
7	0	1	0	1	1	0	1	0	1	0	0	1	3Vdc+Va
8	0	1	0	1	0	1	0	1	1	0	0	1	4Vdc
9	0	1	0	1	0	1	1	0	1	0	0	1	4Vdc+Va
10	0	0	0	0	0	0	0	0	1	0	1	0	0
11	1	0	1	0	1	0	0	1	0	1	1	0	-Vdc
12	1	0	1	0	1	0	1	0	0	1	1	0	-(Vdc+Va)
13	0	1	1	0	1	0	0	1	0	1	1	0	-2Vdc
14	0	1	1	0	1	0	1	0	0	1	1	0	-(2Vdc+Va)
15	0	1	0	1	1	0	0	1	0	1	1	0	-3Vdc
16	0	1	0	1	1	0	1	0	0	1	1	0	-(3Vdc+Va)
17	0	1	0	1	0	1	0	1	0	1	1	0	-4Vdc
18	0	1	0	1	0	1	1	0	0	1	1	0	-(4Vdc+Va)

In this case, the hybrid modulation approach is applied. A six-level Multilevel Inverter is utilized to demonstrate this concept. There are two sections to the modulation. The large pulses will initially drive the switches in the first module, as shown in Figure 3(a).
It is made up of three square waves, the largest of which has a peak magnitude of (1/3.5) pu and smallest of which has a magnitude of (-1/3.5) pu. In both half cycles, these square waves will be employed to exhibit the needed part of the sinusoidal reference signal.Lower square wave in both the half cycles will be placed as shown in Fig 3(a).Module II performs the modulation followed by the subtraction in sinusoidal reference wave which is shown in Fig 3(b).
The gate pulses for switches Sa1 and Sa2 is obtained by comparing the sinusoidal reference signal and lower square wave. Similarly by comparing other square waves we can obtain gate pulses for other switches in module I.

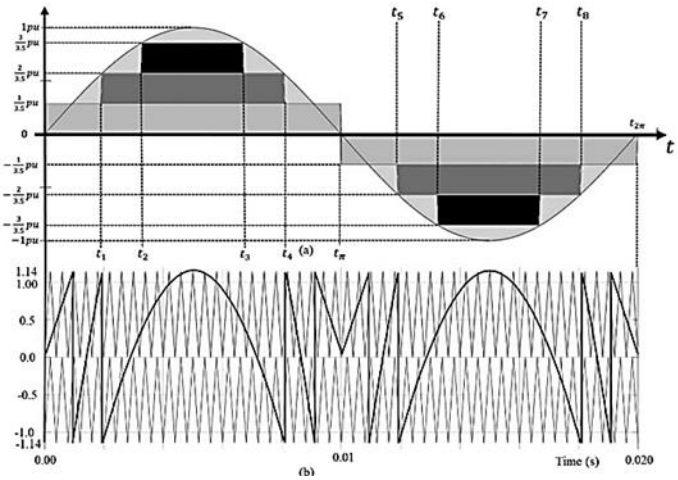

Figure 3: (a) Technique of hybrid modulation (b) Differentiated gate signals, as well as carrier signals

The gate pulses for module II is generated by a differentiated reference signal. his signal is obtained by finding the area which is not common for square waves and sinusoidal reference signal. Afterwards the differentiated signal is differentiated with the carrier signal.

b. Modes of Operation

1 Mode 1

In mode1, the magnitude of dc source in both Modules I and II are equal.

Vam =Vdc

Here we are considering the voltage ,Vdc = 30V.
The number of levels generated at the end of mode 1,

N = 2(m+1)

So here the number of levels generated will be ,

N = 2(3+1)

N = 8

where, m= number of cells in first module 2 Mode 2
To induce more number of level, the magnitude of Vam will be reduced to half of the Vdc value. The dc source value in module I will be same as earlier.
The number of levels obtained at the end of mode 2 ,

N = 4(m+1)+1

So the number of levels obtained will be ,

N = 4(3+1)+1

N = 17

The inverter's total number of IGBT switches,

Nsw = 3(m+2)

Nsw = 15

Less number of switches and dc sources will be employed here than in other systems such as SSPS, CBSC, and so on.

III. SIMULATION MODEL AND RESULT

The simulation is carried out in Simulink as per the design. The mode 1 and mode 2 results are shown in figure 9-12.

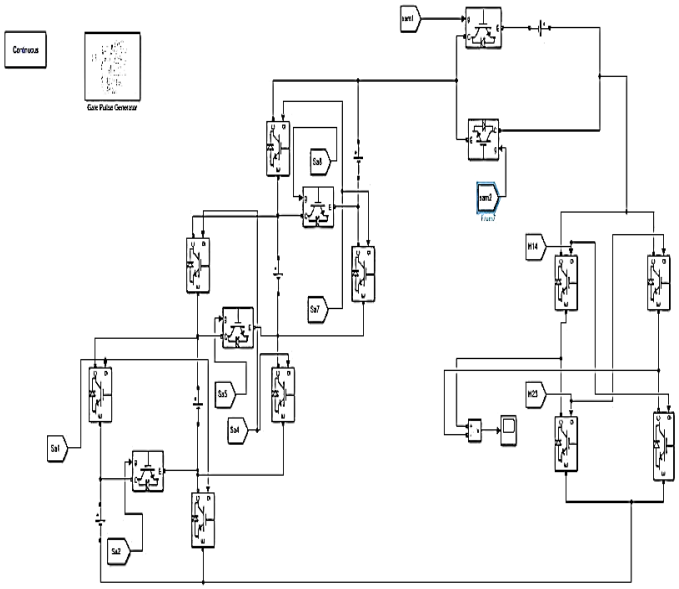

Figure 4: Simulation model of MLI

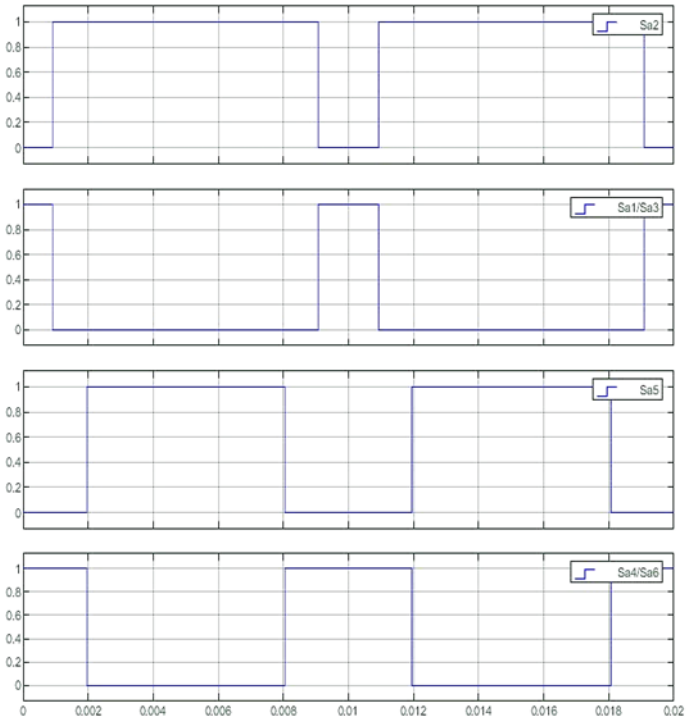

Figure 5: Sa1, Sa2, Sa3, Sa4, Sa5, Sa6 switches gate pulses

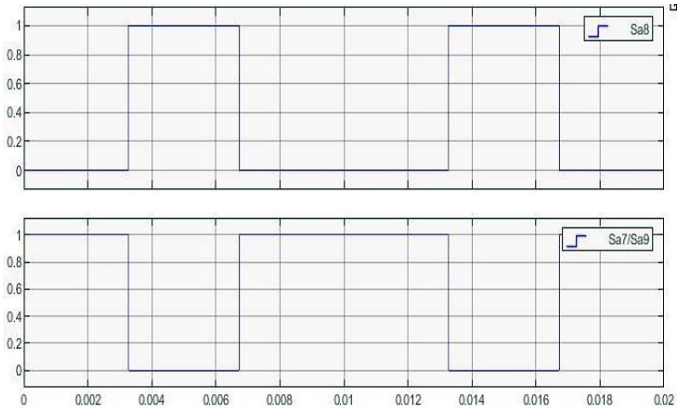

Figure 6: Gate pulses for switches Sa7,Sa8,Sa9

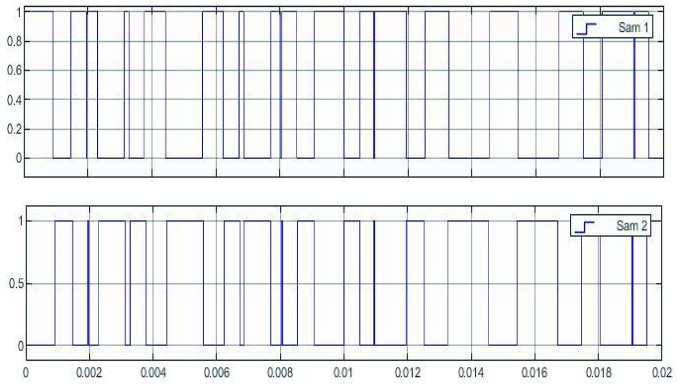

Figure 7: Sam1, Sam2 switches gate pulses

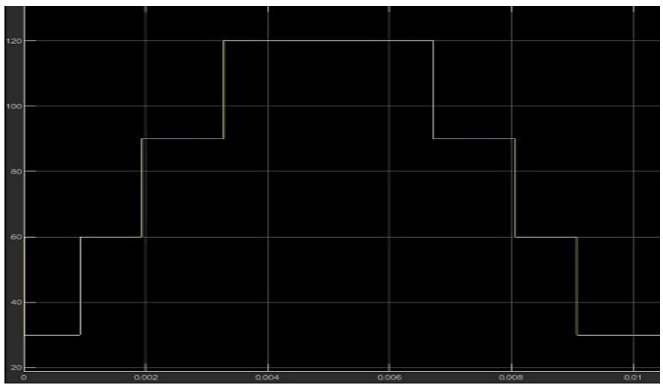

Figure 8: LGM block output

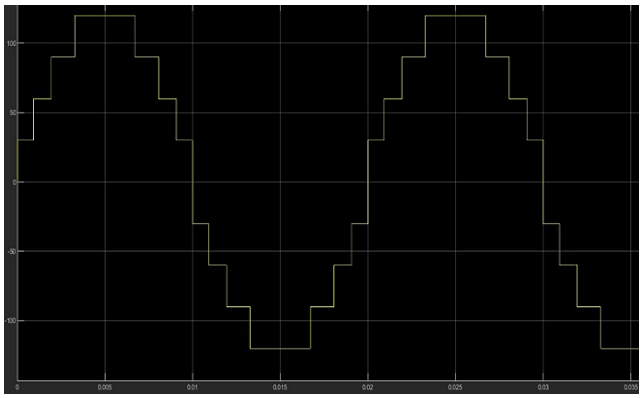

Figure 9: Output voltage waveform of MLI in Mode 1

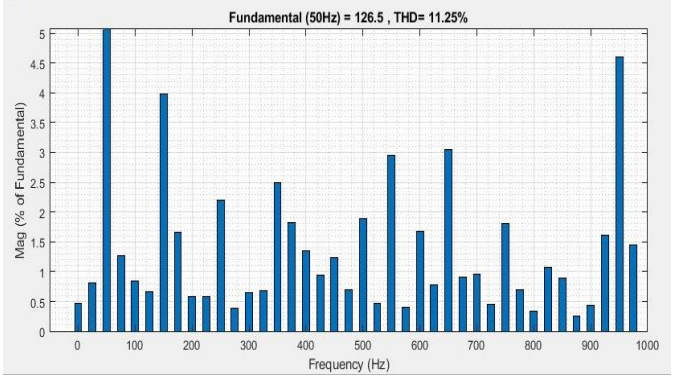

Figure 10:Mode 1 harmonic spectra,THD is 11.25%

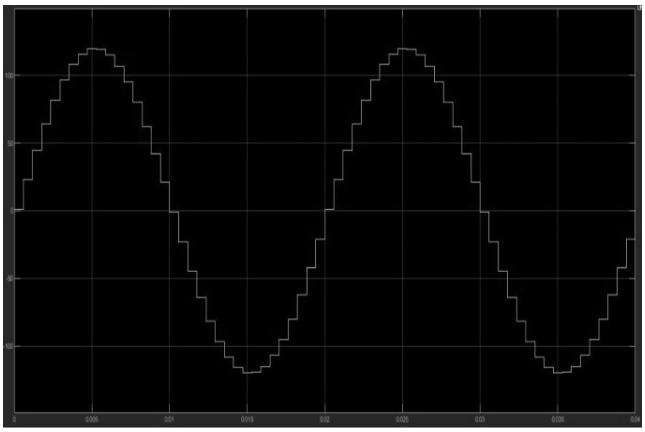

Figure 11: Output voltage waveform of MLI in Mode 2

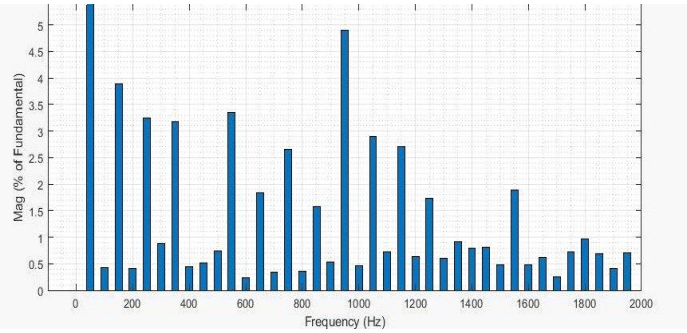

Figure 12: Mode 2 harmonic spectra , THD is 8%

Comparison of THD

Number of levels	Mode 1	Mode 2
13	15.5%	9.5%
17	11.25%	8%

We know that, as the voltage level increases , the harmonic content will decrease and the same can be seen here. Comparing the 13 and 17 level inverter, as the levels are increased, THD value is improved.

IV. CONCLUSION

In this work, the performance of single-phase seventeen level multilevel inverter is discussed by using SIMULINK. As the voltage sources are connected in series/parallel combination load sharing is achieved. Use of hybrid modulation helps in reducing the harmonics and thus reducing the losses and the circuit can be easily handled.

REFERENCES

[1] Vijeh M , Rezanejad M, Samadaei E, Bertilsson K,"A General Review of MLI Based on Main Submodules", IEEE Transaction on Power Electronics, Vol. 34, Issue 10, pp.9479-9502, 2019.

[2] W.Abd Halim, S.Ganeson, M.Azri, Tengku Azam,"Review of Multilevel Inverter Topologies and its Applications", Journal of Telecommunication, Electronics and Computer Engineering, Vol. 8, Issue. 7, pp. 51-56, 2016.

[3] Hussain M. Bassi,"A Modulation Scheme for Floating Source MLI Topology with Increased Number of Output Levels",International Journal of Electrical and Computer Engineering, Vol. 6, Issue 5, pp. 1985-1993, 2016.

[4] Krishna Kumar, Alekh Ranjan, Pallavee, Lalit, and Shailendra, "Multilevel Inverter Topologies with Reduced Device Count: A Review", IEEE Transaction on Power Electronics,Vol.3, Issue 1, pp. 135-151, 2016.

[5] Youhei Hinago and Hirotaka Koizumi,"A Single-Phase Multilevel Inverter Using Switched Series/Parallel DC Voltage Sources", IEEE Transaction on Industrial Electronics,Vol.57, Issue 8, pp. 2643-2650, 2010.

[6] Won-Kyun Choi and Feel-soon Kang,"H-bridge based Multilevel Inverter using PWM Switching Function" INTELEC-2009.

[7] Ebrahim Babaei, "A Cascaded Multilevel Inverter Topology with Reduced Number of Switches", IEEE Transaction on Power Electronics, Vol 23, Issue 6, pp. 2657-2664, 2008.

[8] S H Kang and F S Lee, "A new structure of H-bridge Multilevel inverter", In Proceeding of the Annual Fall Conference of Power Electronics, Goyang, Korea, pp. 388-390, 2008.

[9] José Rodríguez, Jih-Sheng Lai and Fang Zheng Peng "Multilevel inverter,"A Survey of Topologies, Controls and Applications" IEEE Transaction on Industrial Electronics,Vol.49, Issue 4, pp.724-738, 2002.

[10] Javad Ebrahimi and Ebrahim Babaei,"A New Multilevel Converter Topology with Reduced Number of Power Electronic Components", IEEE Transaction on Industrial Electronics,Vol.59, Issue 2, pp.655-667, 2012.

[11] J I Leon, S Vazquez and S Kouro,"Unidimensional modulation technique for cascaded multilevel converters" IEEE Transaction on Industrial Electronics,Vol.56, Issue 8, pp. 2981-2986, 2009.

[12] K K Gupta and S Jain,"Topology for Multilevel Inverter to attain maximum number of levels from given DC Sources", IET Power Electronics, Vol.5, Issue 4, pp. 435-446, 2012.